We claim:

1. A circuit for modeling a course delay element with a plurality of fine delay elements, the circuit comprising:

first and second parallel delay paths receiving a clock signal, the first path including a first plurality of delay elements and the second path including a second plurality of delay elements;

a phase detector receiving first and second clock delay signals from the first and second delay paths respectively for detecting a phase difference between said first and second clock delay signals, the phase detector providing the phase difference to a counter; and

a decoder receiving a signal from the counter, the decoder being connected to the first plurality of delay elements within the first delay path for adjusting the delay provided by the first delay path until the first and second clock delay signals are in a locked state.

2. The circuit according to claim 1 wherein the first plurality of delay elements comprise programmable delay elements.

3. The circuit according to claim 1 wherein the first plurality of delay elements comprise programmable digital delay elements.

4. The circuit according to claim 1 wherein the second plurality of delay elements comprise the same delay

elements of the first plurality of delay elements in addition to a course delay element.

5. The circuit according to claim 1 wherein the second delay path comprises at least one coarse delay element.

6. The circuit according to claim 1 wherein the second delay path comprises at least one coarse delay element in addition to the first delay path.

7. The circuit according to claim 2 wherein the first delay path consists of fine delay elements.

8. The circuit according to claim 1 wherein the phase detector comprises a flip-flop circuit.

9. The circuit according to claim 1 wherein the counter is a count-up count-down type counter.

10. The circuit according to claim 1 further comprising a Delay Lock Loop (DLL), the DLL including a coarse delay line receiving a system clock, a fine delay line coupled to the output of the coarse delay line, the fine delay line providing a delay clock signal; a main phase detector receiving the system clock and the delay clock signal, the phase detector coupled to a main fine counter, the main fine counter adjusting the fine delay line.

11. The circuit according to claim 10 wherein the counter is coupled to the main fine counter.

12. The circuit according to claim 11 wherein a signal provided by the counter to the main fine counter is equivalent to the number of fine delay elements within the fine delay line that correspond to a course delay element within the coarse delay line.

13. A circuit for modeling a course delay element with a plurality of fine delay elements, the circuit including:

(a) first and second parallel delay paths receiving a clock signal, the first path comprising a first plurality of delay elements and the second path including a second plurality of delay elements;

(b) a phase detector receiving a first and second clock delay signals from the first and second delay paths respectively for detecting a phase difference between said first and second clock delay signals, the phase detector providing the phase difference to a counter; and

(c) the counter generating a signal for controlling a plurality of delay elements within the first delay path for adjusting the delay provided by the first delay path until the delay provided by the first and second paths are substantially equal.

14. The circuit according to claim 13 wherein the first plurality of delay elements comprise programmable delay elements.

15. The circuit according to claim 13 wherein the first plurality of delay elements comprise programmable digital delay elements.

16. The circuit according to claim 13 wherein the second plurality of delay elements comprise the same delay elements of the first plurality of delay elements in addition to a course delay element.

17. The circuit according to claim 13 wherein the second delay path comprise at least one coarse delay element.

18. The circuit according to claim 13 wherein the second delay path comprise at least one coarse delay element in addition to the first delay path.

19. The circuit according to claim 13 wherein the first delay path consists of fine delay elements.

20. The circuit according to claim 13 wherein the phase detector comprises a flip-flop circuit.

21. The circuit according to claim 13 wherein the counter is a count-up count-down type counter.

22. The circuit according to claim 13 further comprising a Delay Lock Loop (DLL), the DLL including a coarse delay

line receiving a system clock, a fine delay line coupled to the output of the coarse delay line, the fine delay line providing a delay clock signal; a main phase detector receiving the system clock and the delay clock signal, the phase detector coupled to a main fine counter, the main fine counter adjusting the fine delay line.

23. The circuit according to claim 22 wherein the counter is coupled to the main fine counter.

24. The circuit according to claim 23 wherein a signal provided by the counter to the main fine counter is equivalent to the number of fine delay elements within the fine delay line that correspond to a course delay element within the coarse delay line.

25. A delay lock loop (DLL) comprising a circuit for modeling a coarse delay element with a plurality of fine delay elements, the circuit comprising:

(a) first and second parallel delay paths receiving a clock signal, the first path including a first plurality of delay elements and the second path including a second plurality of delay elements;

(b) a phase detector receiving first and second clock delay signals from the first and second delay paths respectively for detecting a phase difference between said first and second clock delay signals, the phase detector providing the phase difference to a counter; and

(c) the counter generating a signal for controlling a plurality of delay elements within the first delay path for adjusting the delay provided by the first delay path until the first and second clock delay signals are in a locked state.

26. A delay lock loop (DLL) comprising a circuit for modeling a coarse delay element with a plurality of fine delay elements, the circuit comprising:

(a) first and second parallel delay paths receiving a clock signal, the first path including a first plurality of delay elements and the second path including a second plurality of delay elements;

(b) a phase detector receiving a first and second clock delay signal from the first and second delay paths respectively for detecting a phase difference between said first and second clock delay signal, the phase detector providing the phase difference to a counter; and

(c) the counter generating a signal for controlling a plurality of delay elements within the first delay path for adjusting the delay provided by the first delay path until the delay provided by the first and second paths are substantially equal.